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CHI MEI OPTOELECTRONICS CORP.

Issue Date:May.09.2008
Model No.: V470H1-L05
Approval

TFT LCD Approval Specification

MODEL NO.: V470H1 - L05

Customer: _____

Approved by:_____

Note:

Approved By	TV Head Division
	LY Chen

Reviewed By	QRA Dept.	Product Development Div.
	Tomy Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.
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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver.1.0	Jan.17'08	All	All	Preliminary Specification was first issued.
Ver.2.0	Feb.01'08	26	7.2	Update color chromaticity (Rx,Ry,Gx,Gy,By)
	Feb.01'08	26	7.2	Update contrast ratio (Min)
	Feb 01'08	33,34,35	11	Update mechanical characteristics
	Feb 01'08	12	3.2.2	Update electrical specification section drawing
Ver.2.1	Mar 10'08	23	6.1	Input signal timing specifications
	Mar 24'08	5	1.4	Update surface treatment
		15	5.1	LVDS Connector type
		11	3.2.2	BL Lamp Voltage BL Starting Voltage Striking Time PWM Dimming range
	Apr.30'08	26	7.2	Gamma
		22	5.4	Update Vertical and Horizontal Active Display Term
	May.09'08	9	3.1	Update the LVDS interface

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

V470H1-L05 is a 47" TFT Liquid Crystal Display module with 20-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display true 16.7M colors (8-bit/color). The inverter module for backlight isn't built-in.

1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (2000:1)
- Fast response time (Gray to gray average 6.5 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 50 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- 180 degree rotation display option
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1039.68(H) x 584.82 (V) (47" diagonal)	mm	(1)
Bezel Opening Area	1049 (H) x 593 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.5415 (H) x 0.1805 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating /Haze 25%/ 3H	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

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1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	1094.5	1096.0	1097.5	mm	(1), (2)
	Vertical (V)	638.5	640.0	641.5	mm	
	Depth (D)	47.1	48.1	49.1	mm	
Weight		-	14620	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ELECTRICAL ABSOLUTE RATINGS

2.1.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	14.0	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.2 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

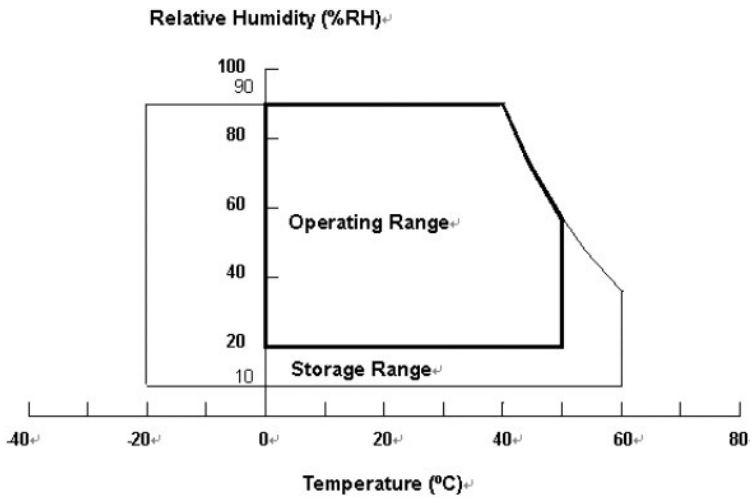
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



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2.3 RELIABILITY TEST CONDITION

No	Test Item	Codition
1	High temperature storage test	Ta = 60℃, 240hrs
2	Low temperature storage test	Ta = -20℃, 240hrs
3	High temperature high humidity storage test	Ta = 50℃, 90%RH, 240hrs
4	High temperature operation test	Ta = 50℃, 240hrs
5	Low temperature operation test	Ta = 0℃, 240hrs
6	High temperature high humidity operation test	Ta = 50℃, 80%RH, 240hrs
7	Vibration test (non-operation)	Wave form: Sine wave Vibration level: 1.0G Fre. range : 10~200Hz Duration: X, Y, Z, 10min, One time each direction
8	Shock test (non-operation)	Wave form: half sine wave Shock level: 50G ±X, ±Y, ± Z, 11ms One time each direction

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3. ELECTRICAL CHARACTERISTICS

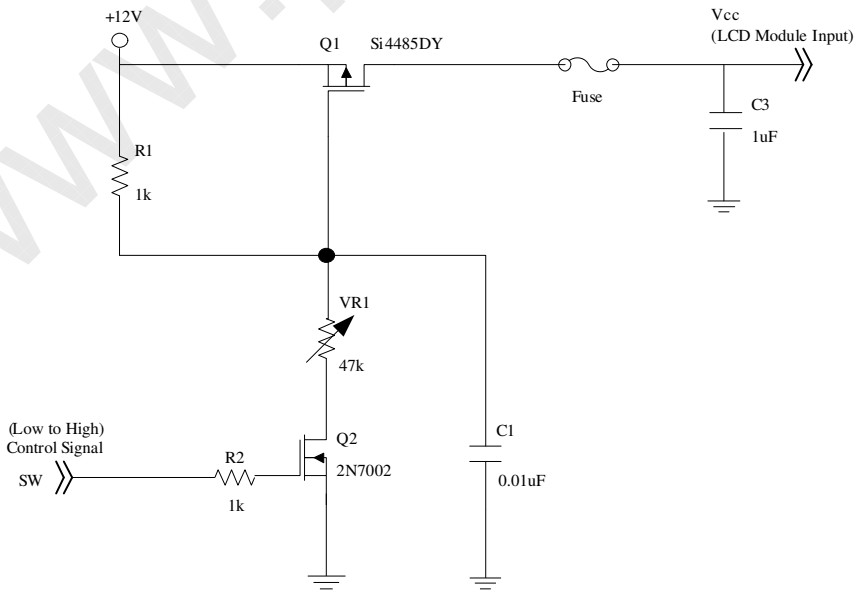
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCC	10.8	12	13.2	V	(1)
Power Supply Ripple Voltage		VRP	-	-	350	mV	
Rush Current		IRUSH	-	-	4.5	A	(2)
Power Supply Current	White Pattern	- - -	-	1.4	1.7	A	(3)
	Mosaic Pattern		-	1.0	-	A	
	Black Pattern		-	0.5	-	A	
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	100	-	-	mV	
	Differential Input Low Threshold Voltage	VLVTL	-	-	-100	mV	
	Common Input Voltage	VLVC	1.07	1.25	1.375	V	
	Terminating Resistor	RT	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



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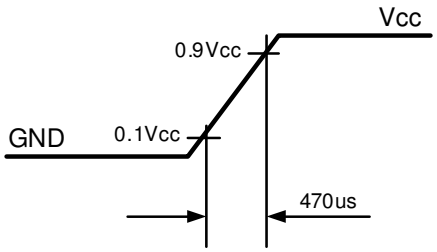
Vcc rising time is 470us

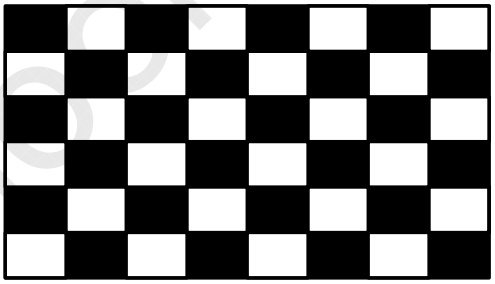


Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, fv = 50 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Mosaic Pattern



Active Area

c. Black Pattern

Active Area

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3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 LAMP SPECIFICATION

(Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Starting Voltage	VSL	-	-	2600	VRMS	Ta = 0 ºC
		-	-	2350	VRMS	Ta = 25 ºC
Lamp Voltage	VL	1503	1670	1837	VRMS	
Lamp Current	IL	5.5	6.0	6.5	mARMS	
Lamp Frequency	FL	40	-	80	KHz	
Lamp Life Time	LBL	50,000	60,000	-	Hrs	(1)

Note(1) Condition: PWM 100% dimming duty ratio

3.2.2 ELECTRICAL SPECIFICATION

(Ta = 25 ± 2 ºC, 100% dimming duty ratio)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
BL Starting Voltage	VSBL	1640			VRMS	(1), Ta = 0 ºC
		1543			VRMS	(1), Ta = 25 ºC
BL Lamp Voltage	VBL	1000	1300	1600	VRMS	
BL Lamp Current	IBL	115	125	135	mARMS	20 lamps
BL Lamp Frequency	FBL	43	45	47	KHz	
PWM Dimming Range	PDIM	10	-	100	%	(2)
Striking Time	ST	1.5	-	-	Sec	
Lamp Type	-	Straight Type			-	
Number of Lamps	-	20			PCS	
Type of Current Balance	-	C-Balance			-	
C Ballaster	CB	-	22	-	pF	

Note (1) Single size values and $VSBL=[(VSL/2)^2+VC^2]^{1/2}$

Note (2) V470H1-L05 are designed without Inverter. These items are for reference and based on V470H1-L03 Inverter model.

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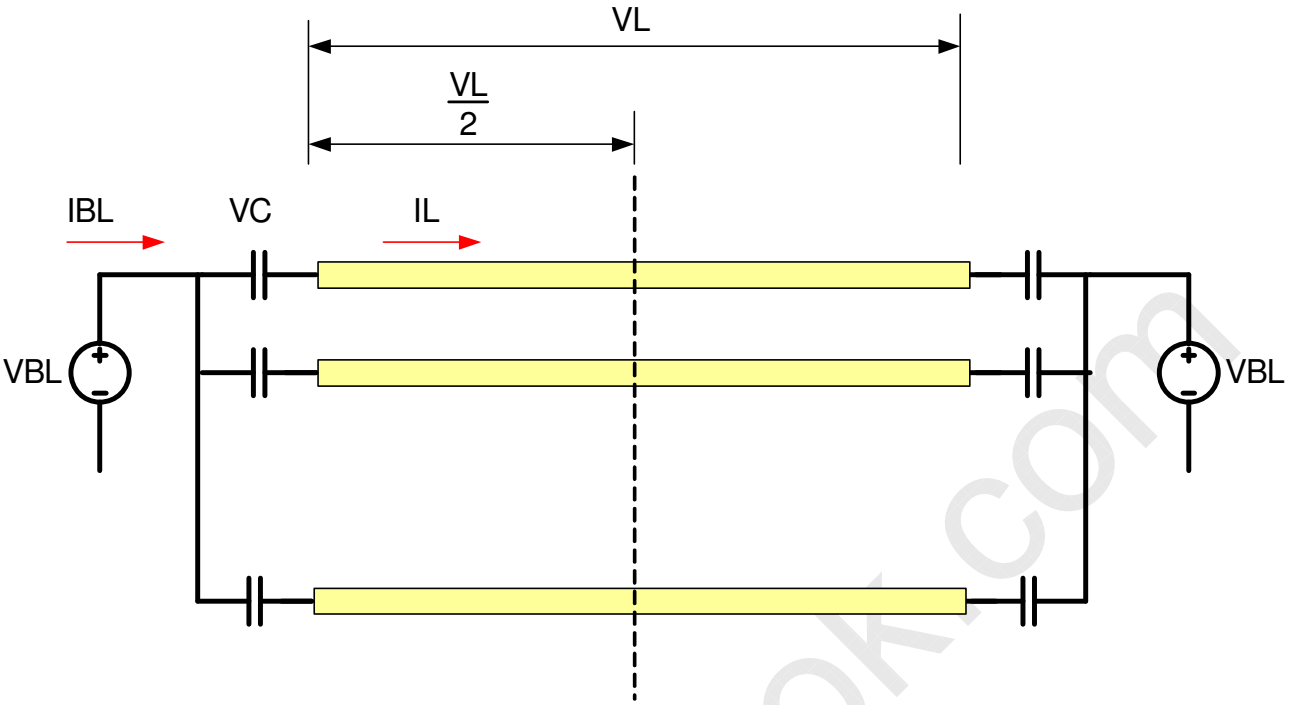

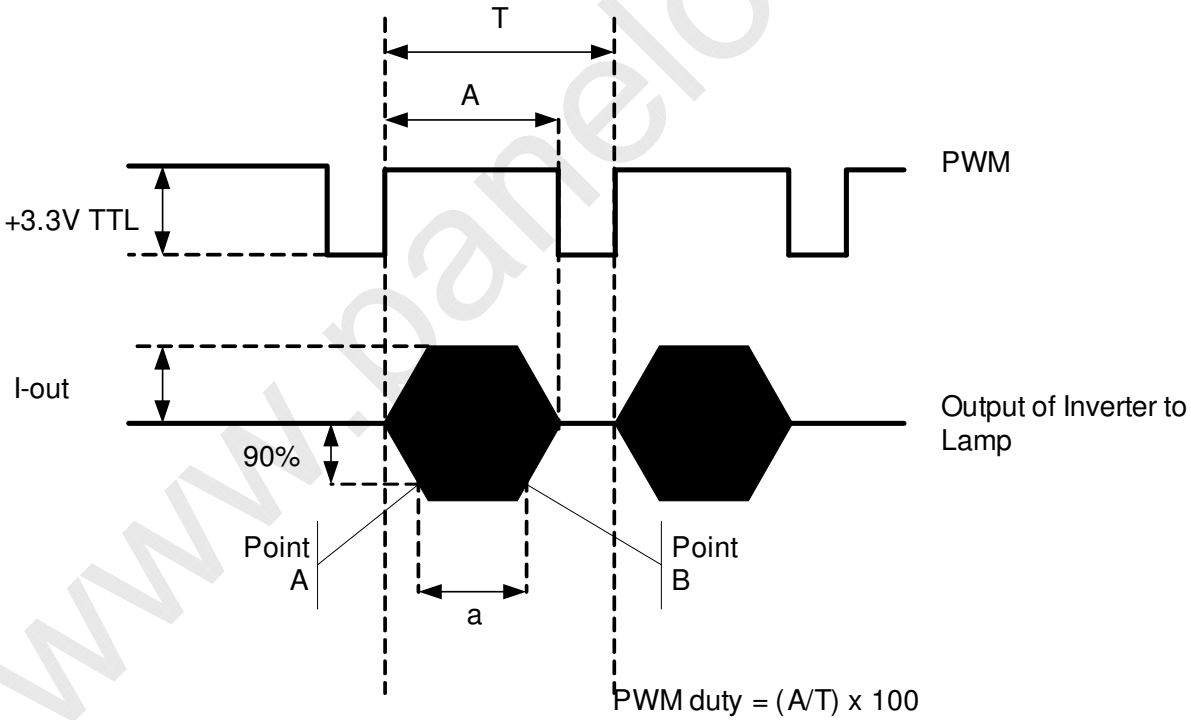

PWM duty = (A/T) x 100
Point A, B: 90% of I-out point
I-out duty = (a/T) x 100
PWM Frequency = 1/T
Note: 20% PWM dimming is around 20% luminance

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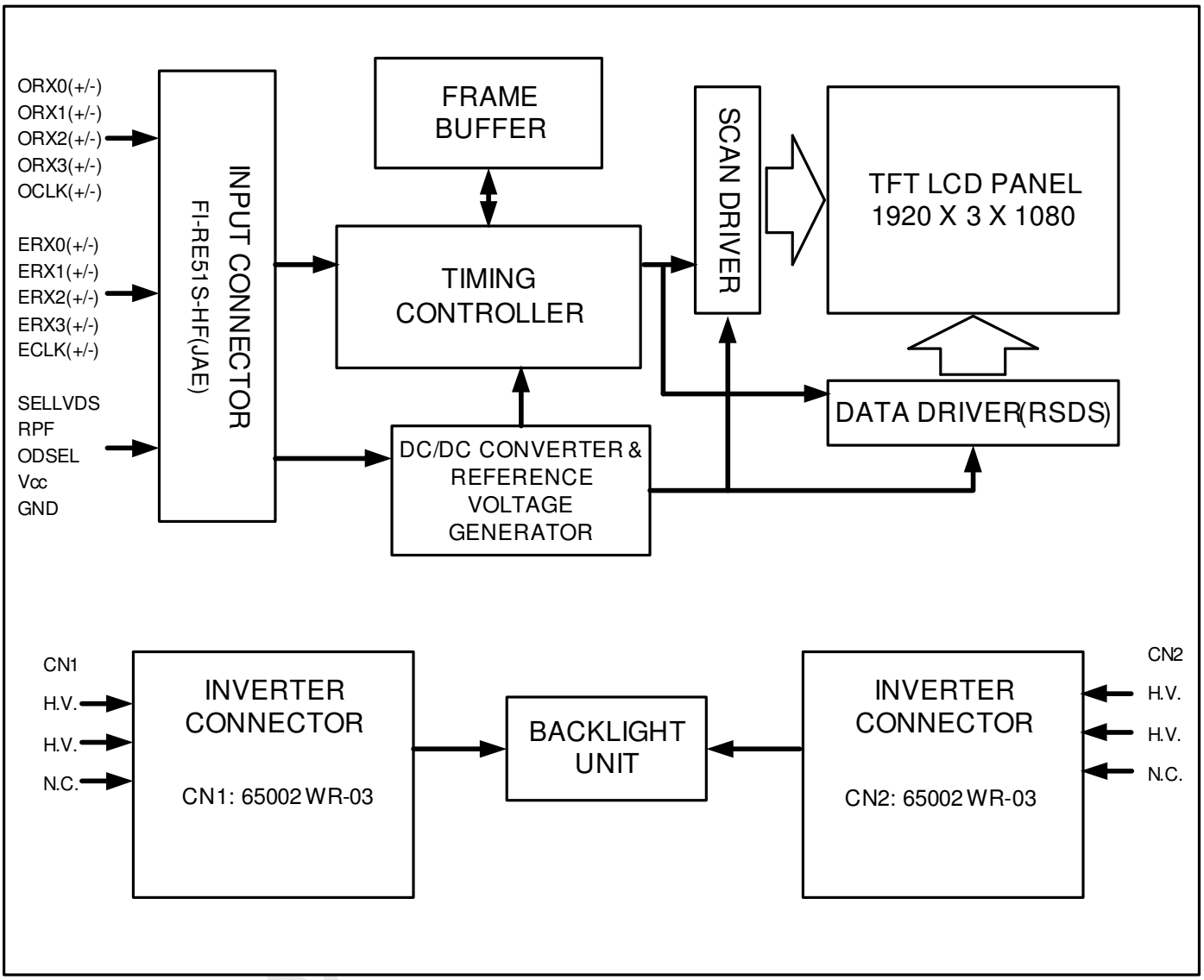
4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



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5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

LSGT05L (LG)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	Low : VESA Format (Default), High : JEIDA Format	(3)
8	RPF	Display Rotation	(2)
9	Reserved	Reserved	
10	Reserved	Reserved	
11	Reserved	Reserved	
12	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	
13	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel Negative LVDS differential clock input.	
20	OCLK+	Odd pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	
23	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	
25	N.C.	No Connection	
26	N.C.	No Connection	
27	N.C.	No Connection	

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28	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	
29	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
30	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel Negative LVDS differential clock input.	
36	ECLK+	Even pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	
39	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	
41	N.C.	No Connection	
42	N.C.	No Connection	
43	N.C.	No Connection	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	GND	Ground	
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) Reserved for internal use. Please leave it open.

Note (2) Low : normal display (Default), High : display with 180 degree rotation.

Normal Display

180° Rotation Display

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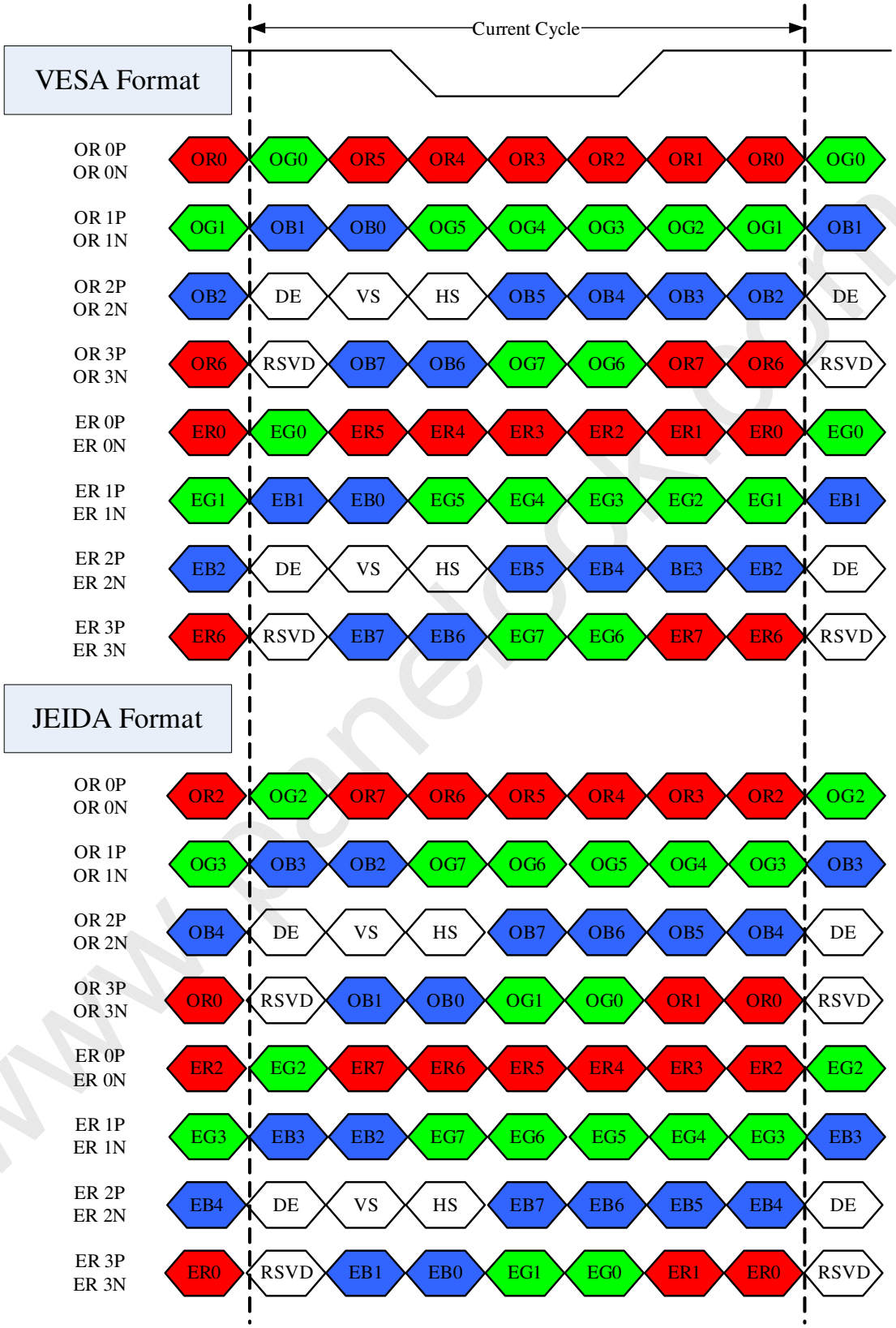
Note (3) LVDS Format:



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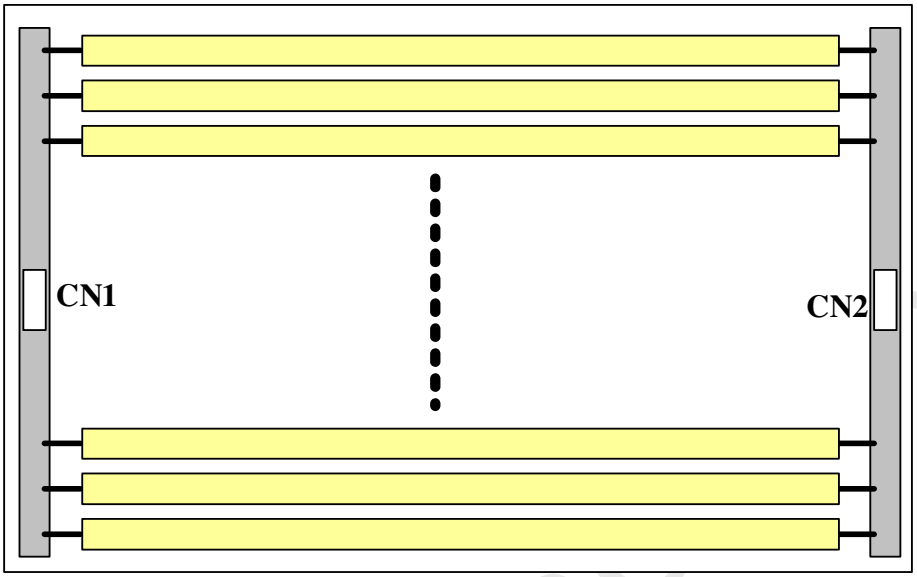
5.2 BACKLIGHT UNIT

CN1-CN2: 65002WR-03.

Pin	Symbol	Description
1	H.V.	High Voltage for Backlight Unit
2	H.V.	High Voltage for Backlight Unit
3	N.C.	No Connection



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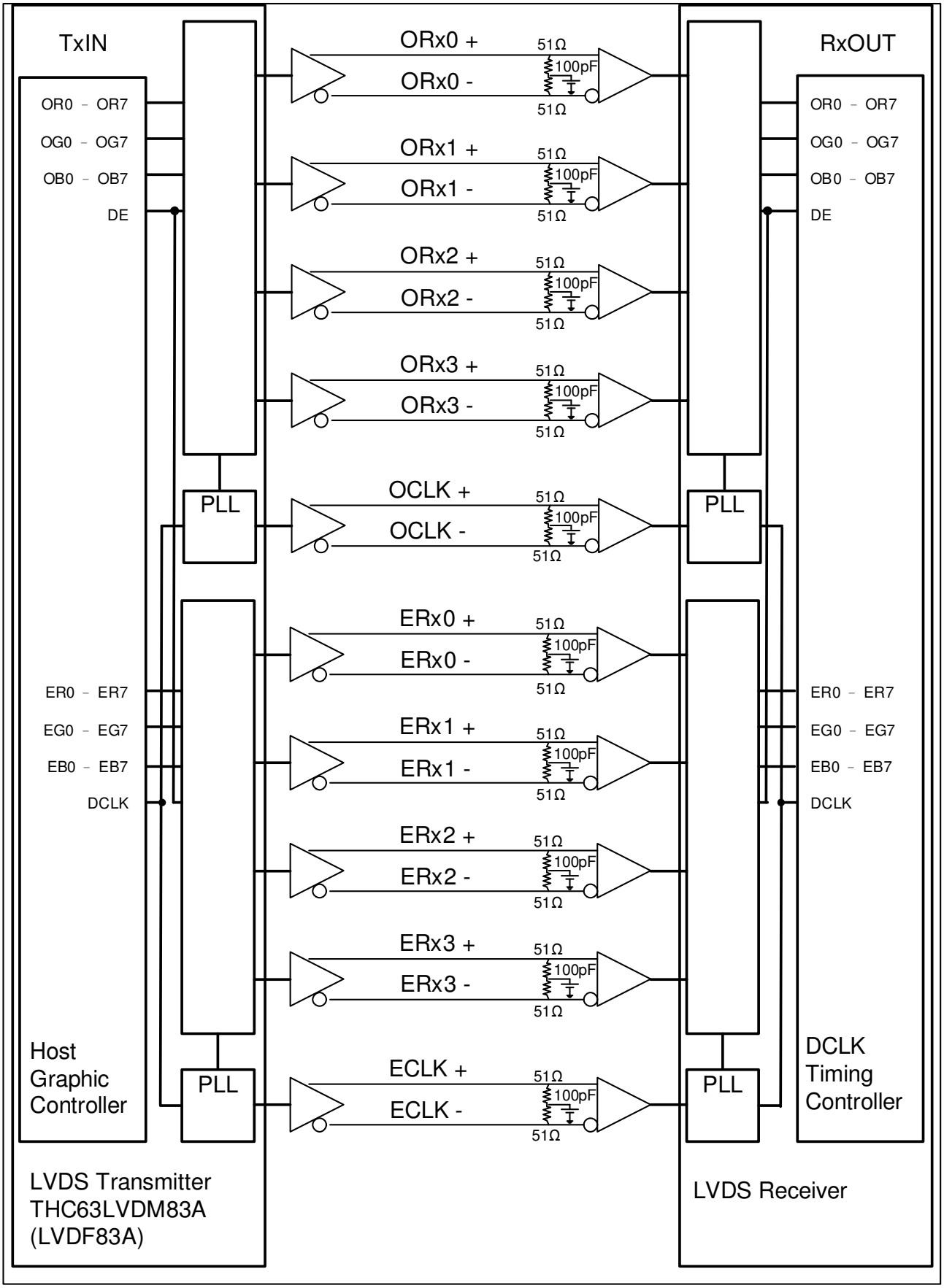
5.3 BLOCK DIAGRAM OF INTERFACE



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OR0~OR7: Odd pixel R data

OG0~OG7: Odd pixel G data

OB0~OB7: Odd pixel B data

ER0~ER7: Even pixel R data

EG0~EG7: Even pixel G data

EB0~EB7: Even pixel B data

DE: Data enable signal

DCLK: Data clock signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

Note (3) Two pixel data send into the module for every clock cychle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

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5.4 LVDS INTERFACE

	SIGNAL		TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
	LVDS_SEL =L or OPEN	LVDS_SEL = H	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	LVDS_SEL =L or OPEN	LVDS_SEL = H
24 bit	R0	R2	51	TxIN0			27	Rx OUT0	R0	R2
	R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
	R2	R4	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2	R4
	R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
	R4	R6	56	TxIN4			33	Rx OUT4	R4	R6
	R5	R7	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5	R7
	G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
	G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
	G2	G4	7	TxIN9			39	Rx OUT9	G2	G4
	G3	G5	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3	G5
	G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
	G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
	B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
	B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
	B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
	B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
	B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
	B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
	DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
	R6	R0	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6	R0
	R7	R1	2	TxIN5			34	Rx OUT5	R7	R1
	G6	G0	8	TxIN10			41	Rx OUT10	G6	G0
	G7	G1	10	TxIN11			42	Rx OUT11	G7	G1
	B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
	B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
	RSVD 1	RSVD 1	25	TxIN23			2	Rx OUT23	NC	NC
	RSVD 2	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	NC	NC
	RSVD 3	RSVD 3	28	TxIN25			5	Rx OUT25	NC	NC
	DCLK		31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK	

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

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5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red Gray Scale	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green Gray Scale	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue Gray Scale	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

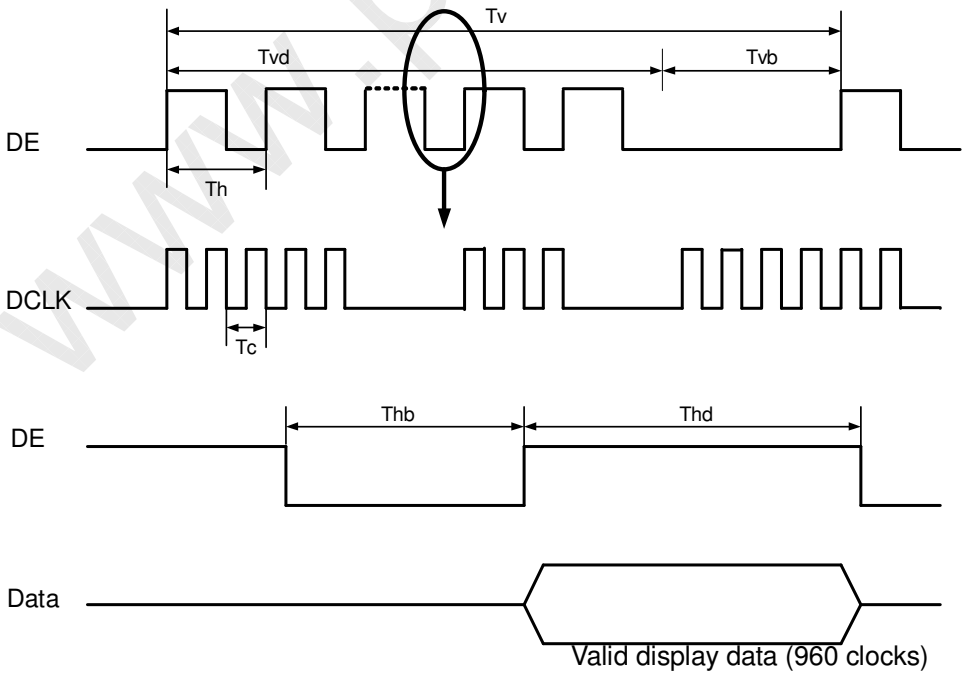
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74	80	MHZ	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate		47	50	63	Hz	
	Total	Tv	1100	1125	1250	Th	(2) Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	20	45	170	Th	-
Horizontal Active Display Term	Total	Th	1050	1100	1290	Tc	(2) Th=Thd+Thb
	Display	Thd	960	960	960	Tc	-
	Blank	Thb	90	140	330	Tc	-

Note(1): Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note(2) : The LVDS clock frequency can't exceed 80MHz.

INPUT SIGNAL TIMING DIAGRAM



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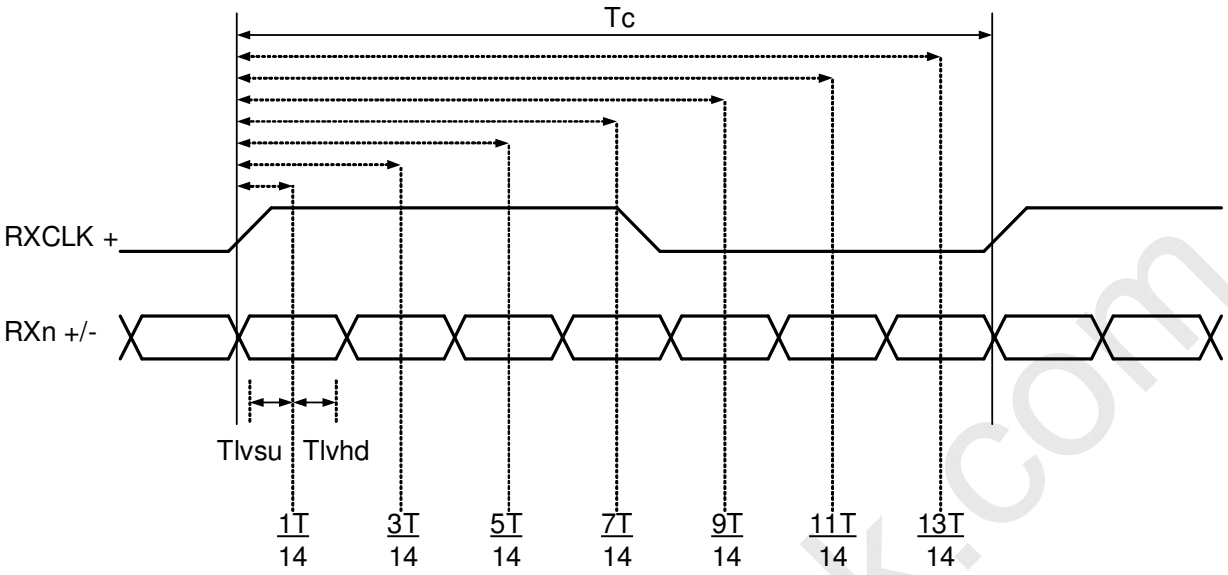
LVDS INPUT INTERFACE TIMING DIAGRAM



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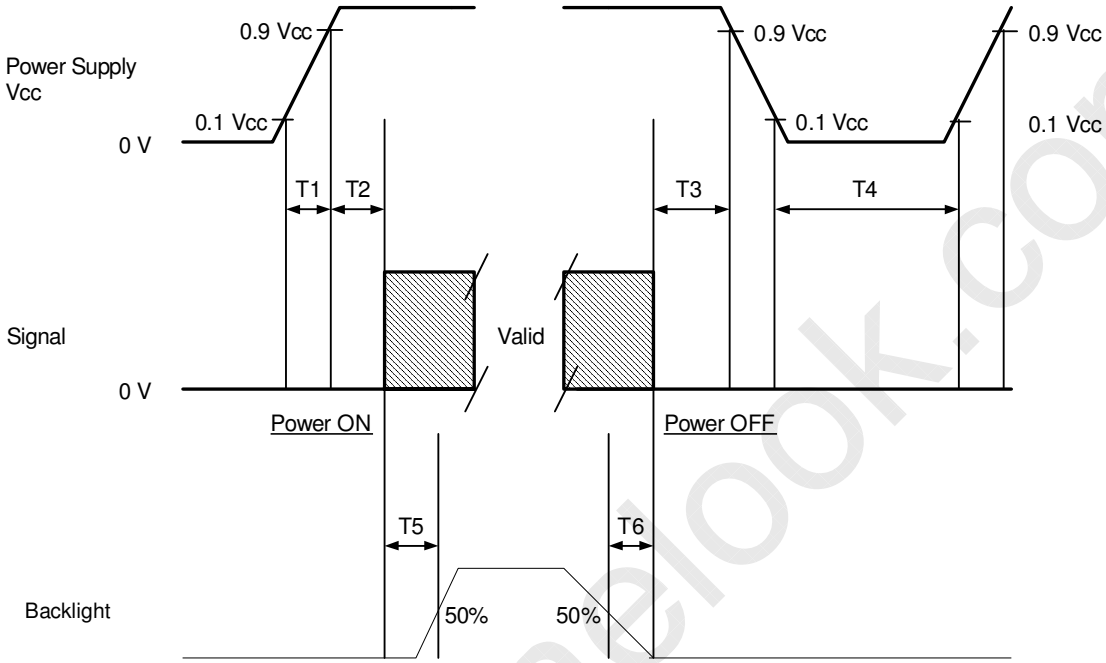
6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.

POWER ON/OFF SEQUENCE



Signal	Min.	Typ.	Max.	Unit	Note
T1	0.5	-	10	ms	-
T2	0	-	50	ms	-
T3	0	-	50	ms	-
T4	500	-	-	ms	-
T5	500	-	-	ms	-
T6	100	-	-	ms	-

Note.

The supply voltage of the external system for the module input should follow the definition of Vcc.

Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

T4 should be measured after the module has been fully discharged between power off and on period.

Interface signal shall not be kept at high impedance when the power is on.

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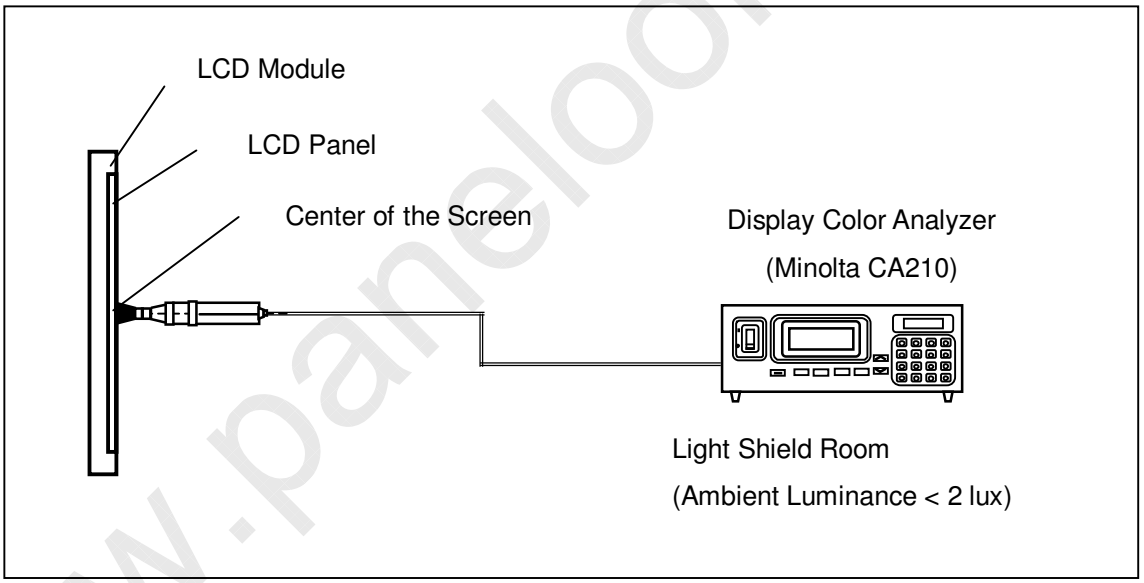
7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	125±10	mA
Oscillating Frequency (Inverter)	FW	45±2	KHz
Vertical Frame Rate	Fr	50	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



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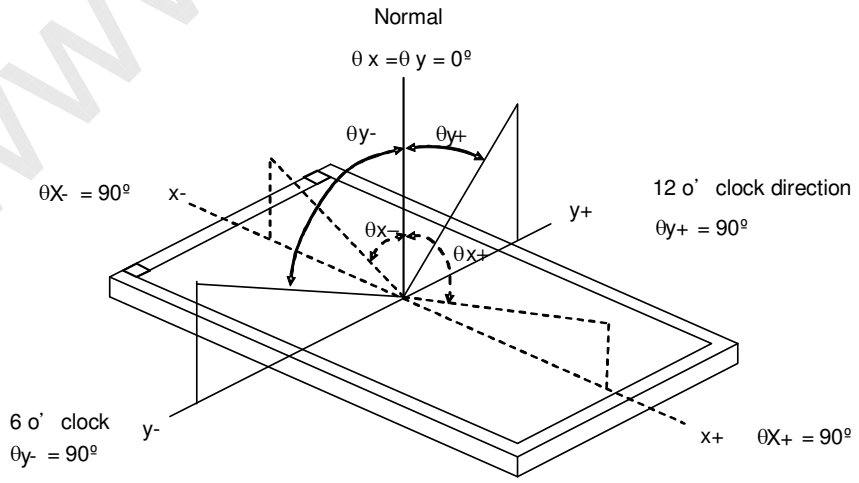
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	(1600)	(2000)		-	Note (2)
Response Time		Gray to gray			(6.5)	(12)	ms	Note (3)
Center Luminance of White		LC		(400)	(500)		cd/m^2	Note (4)
White Variation		δW				(1.3)	-	Note (7)
Cross Talk		CT				(4)	%	Note (5)
Color Chromaticity	Red	Rx		Typ. -0.03	(0.644)	Typ. +0.03	-	Note (6)
		Ry			(0.332)		-	
	Green	Gx			(0.273)		-	
		Gy			(0.597)		-	
	Blue	Bx			(0.143)		-	
		By			(0.069)		-	
	White	Wx			(0.280)		-	
		Wy			(0.285)		-	
	Color Gamut	C.G		(70)	(72)		%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20	80	88		Deg.	Note (1)
		θx-		80	88			
	Vertical	θY+		80	88			
		θY-		80	88			
Gamma				-	2.2	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



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Note (2) Definition of Contrast Ratio (CR):

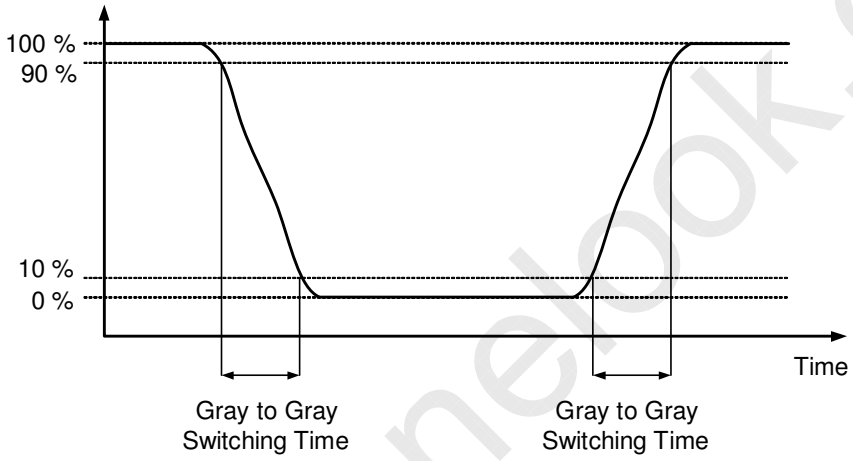
The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray-to-Gray Switching Time:

Optical Response



The driving signal means the signal of luminance 0%, 20%, 40%, 60%, 80%, 100%.

Gray to gray average time means the average switching time of luminance 0%, 20%, 40%, 60%, 80%, 100% to each other.

Note (4) Definition of Luminance of White (LC, LAVE):

Measure the luminance of gray level 255 at center point and 5 points

LC = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (7).

Note (5) Definition of Cross Talk (CT):

CT = | YB – YA | / YA × 100 (%)

Where:

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

YB = Luminance of measured location with gray level 0 pattern (cd/m2)

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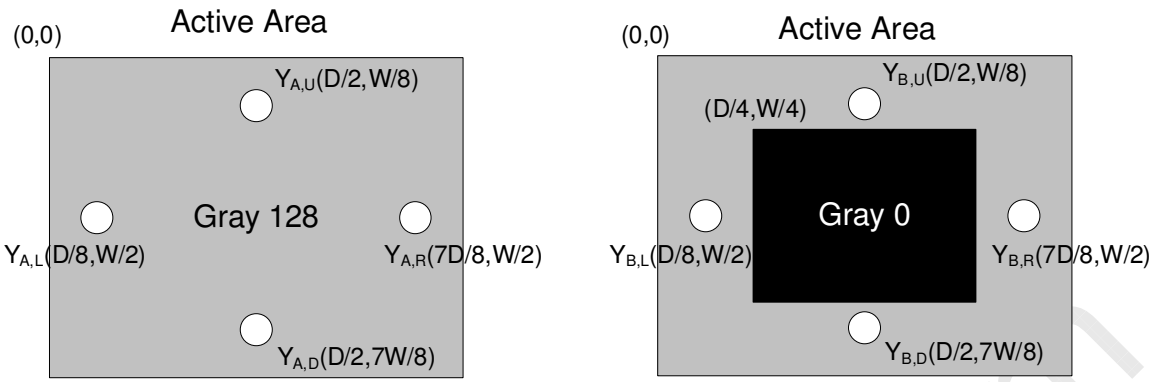
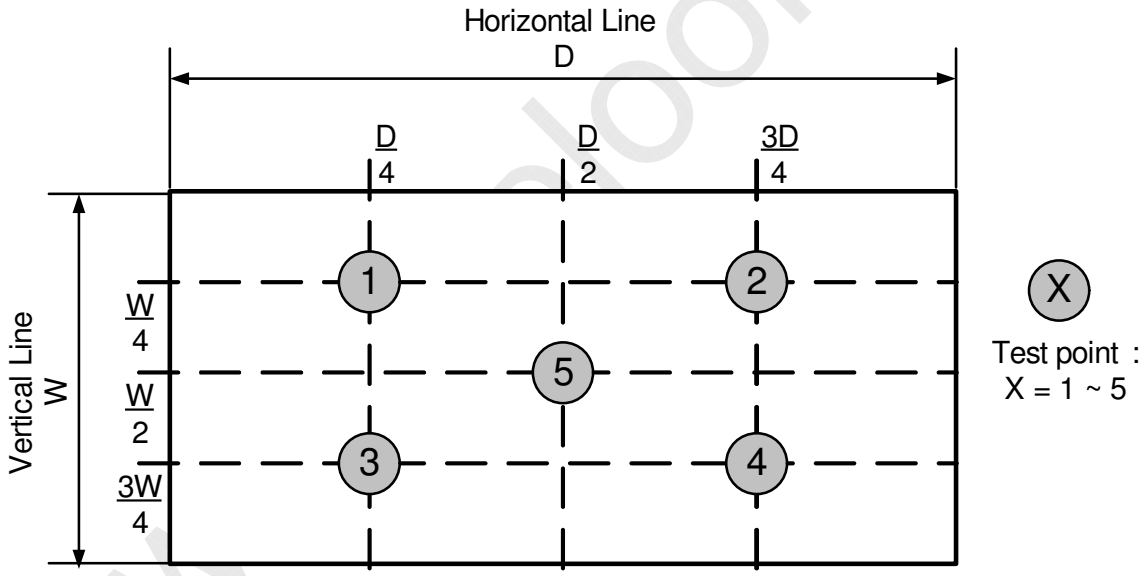


Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



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8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not plug in or pull out the I/F connector while the module is in operation.

[6] Do not disassemble the module.

[7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9] When storing modules as spares for a long time, the following precaution is necessary.

[9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[10] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

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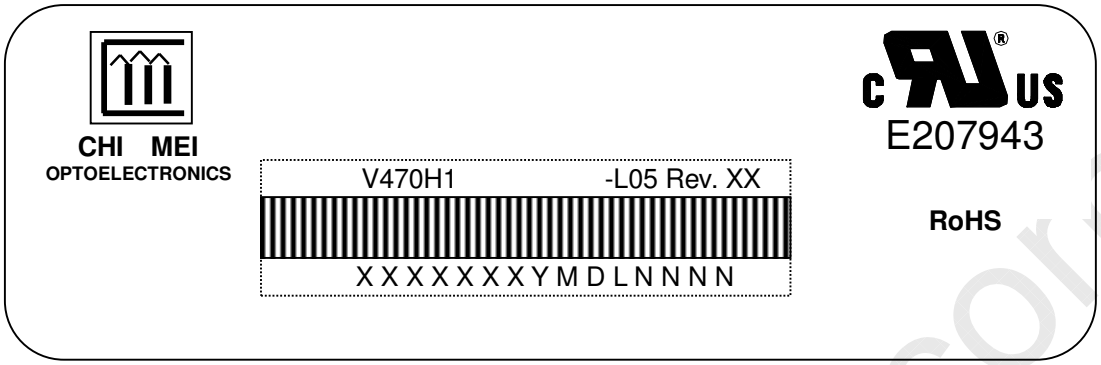
9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

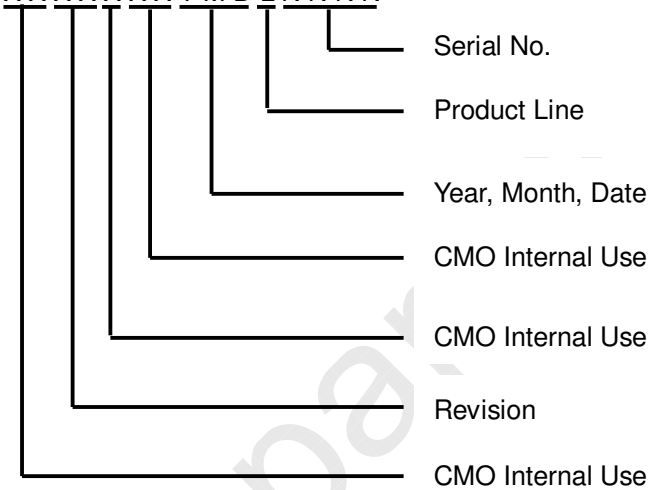
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V470H1-L05

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, …etc.

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10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

3 LCD TV modules / 1 Box

Box dimensions : 1190(L)x280(W)x720(H)mm

Weight : approximately 52Kg (3 modules per box)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method.

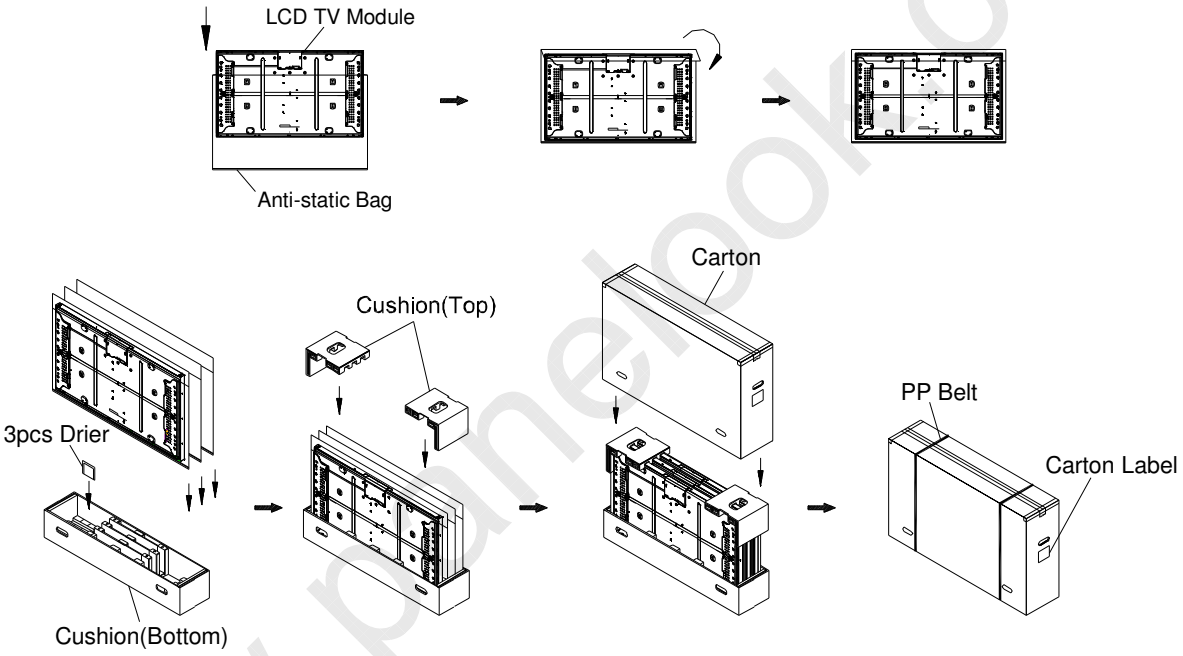

Figure.10-1 packing method

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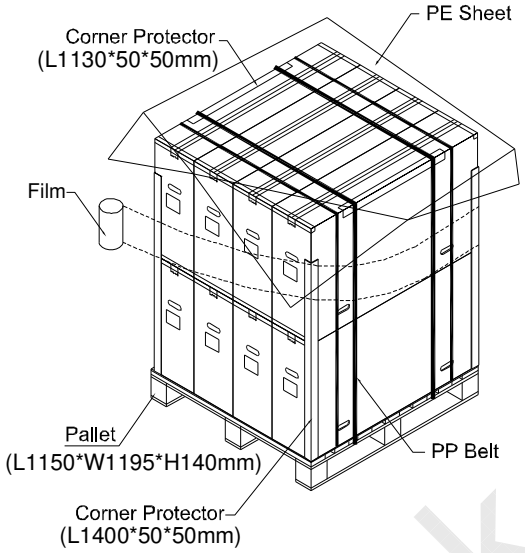
Air Transportation &

Sea / Land Transportation (40ft Container)



Sea / Land Transportation (40ft HQ Container)

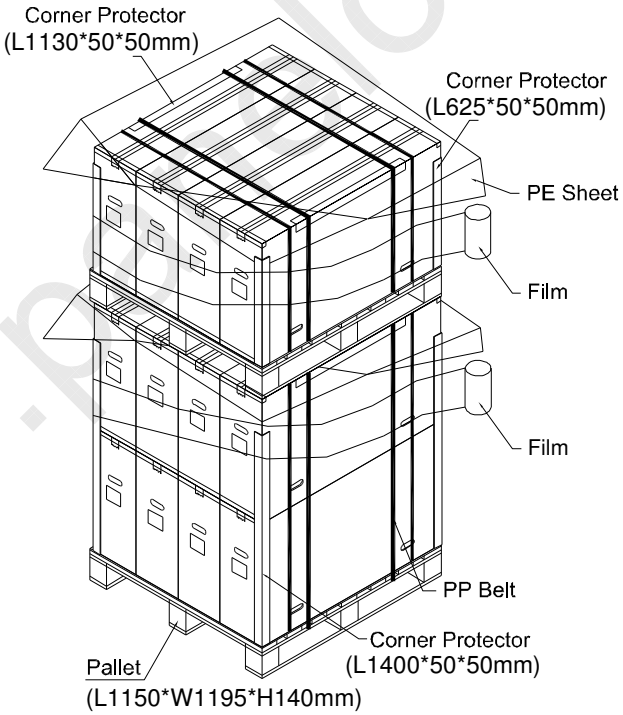


Figure.10-2 Packing method

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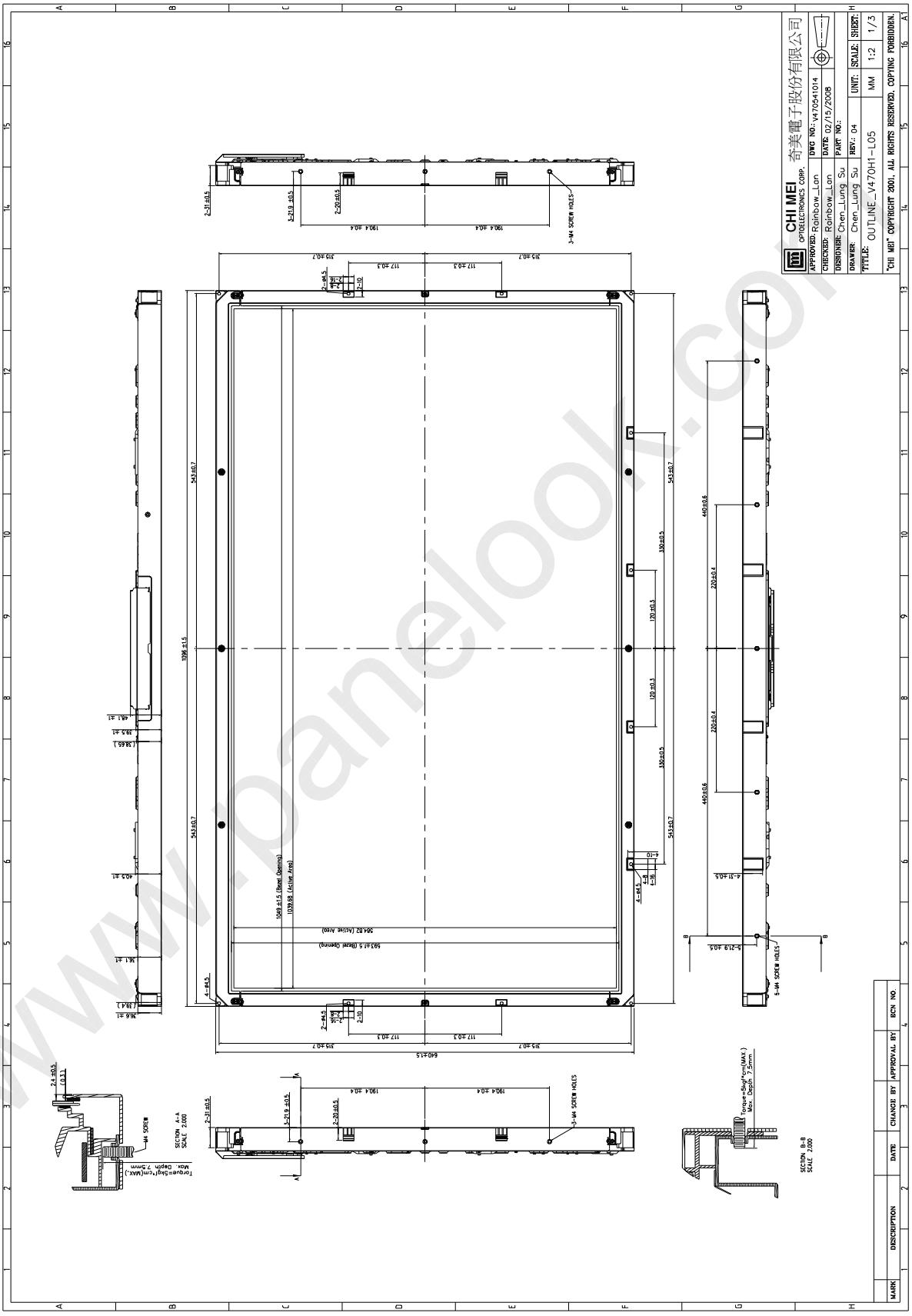
11. MECHANICAL CHARACTERISTICS



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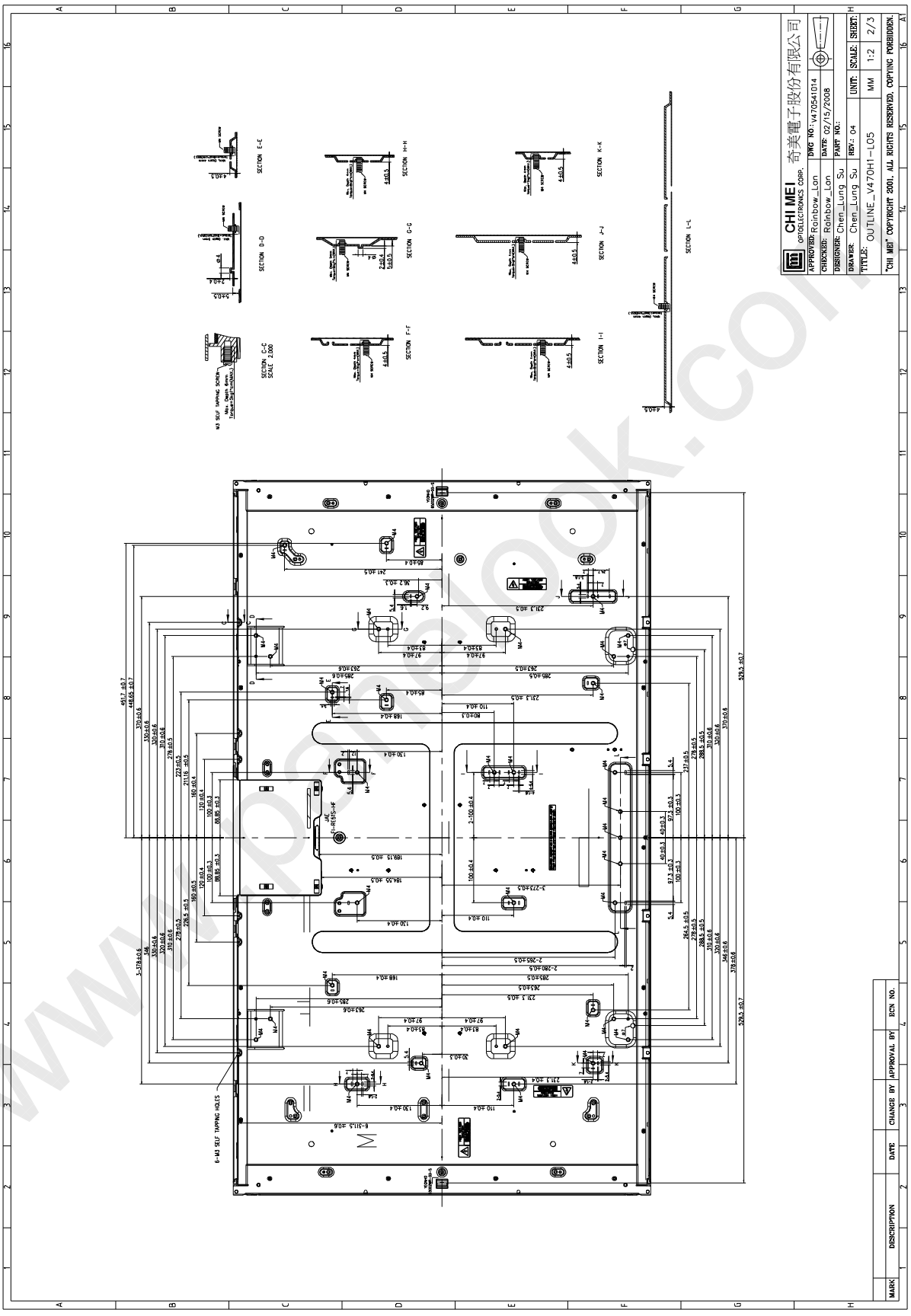

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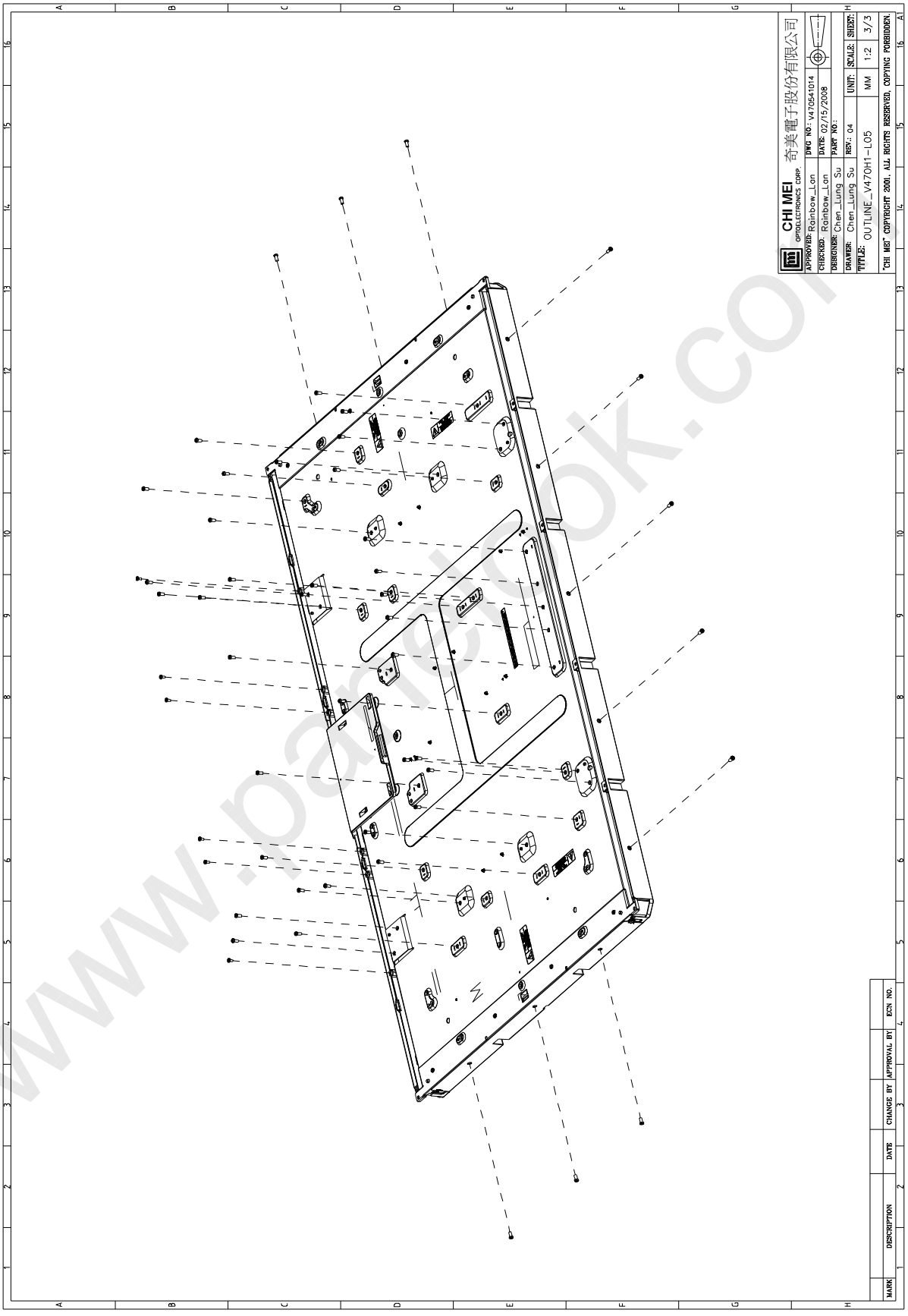

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